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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,372	11/21/2001	Richard H. Lane	M4065.0338/P338-A	1348
24998	7590	09/28/2004	EXAMINER	
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP			DOAN, THERESA T	
2101 L STREET NW			ART UNIT	
WASHINGTON, DC 20037-1526			PAPER NUMBER	
			2814	

DATE MAILED: 09/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/989,372

Applicant(s)

LANE, RICHARD H.

Examiner

Theresa T Doan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07/13/04.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 29-32, 34-39, 41, 44-47, 49 and 51-64 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 29-32, 34-39, 41, 44-47, 49 and 51-64 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 29-32, 34-39, 41,44-47, 49 and 51-64 are rejected under 35 U.S.C. 102(e) as being anticipated by Xing et al. (U.S. 6,090,697) as previously cited.

Regarding claims 29-32 and 34-35, Xing et al. teach in figure 3 a semiconductor device comprising:

a semiconductor substrate 300;

an insulating layer 316 provided over the substrate; and

a platinum metal layer 304 provided within an opening of the insulating layer to form a lower capacitor electrode, wherein the metal layer having a thickness of approximately 100-500 angstroms and wherein a top surface of the metal layer 304 is

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down to the insulating layer so that the top surface of the metal layer 304 is at the same level with a top surface of the insulating layer 316 (see figure 3). It is note that the process limitation (forming by an electro-polished) would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claims 36-39 and 41, Xing et al. teach in figures 3 and 6a, a memory cell comprising:

a transistor (not shown) including a gate fabricated on the semiconductor substrate and including a source/drain region in the semiconductor substrate disposed adjacent to the gate (figure 6a);

a platinum metal layer 304 within an insulating layer 316 provided over the substrate wherein a thickness of approximately 100-500 angstroms (figure 3, column 6, lines 13-17); and

a container capacitor including a lower electrode 304 and a dielectric layer 312 over the lower electrode, the lower electrode having a surface aligned over the source/drain region, the platinum metal layer forming the platinum lower electrode, and the dielectric layer 312 being in contact with the insulating layer 316. It is note that the process limitation (forming by an electro-polished) would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

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Regarding claims 44-47 and 49, Xing et al. teach in figure 3 a processor-based system comprising:

a processor (column 13, lines 14-22); and

an integrated circuit coupled to the processor, at least one of the integrated circuit and processor comprising a container capacitor provided within an insulating layer 316, the container capacitor including a platinum lower electrode 304 having a thickness of approximately 50-300 angstroms (figure 3, column 6, lines 13-17), wherein a top surface of the metal layer 304 is at the same level with a top surface of the insulating layer 316. It is note that the process limitation (forming by an electro-polished) would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claims 51-54, Xing et al. further teach the integrated circuit may be used in DRAMs, FRAMs and other types of integrated circuits (column 3, lines 28-30).

Regarding claims 55-58, Xing et al. teach in figure 3 a container capacitor comprising:

a platinum lower electrode 304 provided within a first insulating layer 316, the platinum lower electrode 304 comprising a metal layer having a bottom wall and vertical sidewalls extending upwardly, wherein the platinum metal layer has a thickness of approximately 100-500 angstroms (figure 3, column 6, lines 13-17); a second insulating layer 312 provided over the metal layer and in contact with the first insulating layer 316;

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and an upper electrode 314 provided over the second insulating layer 312. It is note that the process limitation (forming by an electro-polished) would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 59, Xing et al. teach in figure 3 a container capacitor comprising:
a barrier conductive layer 308.

Regarding claims 60-64, Xing et al. teach in figure 3 a container capacitor comprising: an insulating layer 316 provided over a substrate 300; a plurality of opening provided in the insulating layer; and a plurality of platinum lower capacitor electrodes provided along the bottom and sidewalls of respective ones of the openings, the platinum lower electrodes being formed as discrete metal layers, wherein the platinum electrodes 304 have a thickness of approximately 100-500 angstroms (figure 3, column 6, lines 13-17); and a dielectric layer 312 associated with each of the discrete the platinum lower electrodes, the dielectric layer being in contact with the first insulating layer 316. It is note that the process limitation (forming by an electro-polished) would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

Response to Arguments

Applicant argues that Xing fails to teach a top surface of the electropolished patterned metal layer is down to the insulating layer so that the top surface of the metal layer is at the same level with a top surface of the insulating layer and in contact with the insulating layer. The argument is not persuasive because Xing (in figure 3) teaches that a top surface of the metal layer 304 is down to the insulating layer so that the top surface of the metal layer 304 is at the same level with a top surface of the insulating layer 316 and in contact with the insulating layer (see figure 3).

Applicant argues that “the limitation **electropolished patterned** is simply not a product-by-process limitation, but rather a *resulting structure* having distinct and defined characteristics”. It should be noted that claims 29, 36, 44, 55 and 59-60 are not directed to any method for making a semiconductor device, but rather, are directed to the resulting of a semiconductor device. Therefore, the process limitation recited in claims 29, 36, 44, 55 and 59-60 (forming by an electro-polished) would not carry patentable weight in claims drawn to a structure because these claims are directed to the product, no matter how the product of these claims is actually made, and the patentability of the final product must be determined, not the patentability of the process, which in any case have not been presented in “product by process” claims. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985). Applicant’s argument thus is not persuasive because the final structure of the metal formed by electropolished process as claimed does not distinguish from the final structure of the metal layer of Xing.

Also, Applicant argues that the patterned metal layer formed by “electropolished” process has resulting structure distinct from the resulting structure of the pattern metal layer 304 of Xing. However, Applicant fails to point out which claimed resulting structure is distinct from the resulting structure of the patterned metal layer 304 of Xing.

Applicant's arguments, addressed to the amended claims are considered in the rejections shown above.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Thursday from 8:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TD
September 20, 2004.



PHAT X. CAO
PRIMARY EXAMINER